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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,748	02/19/2004	Kazuhiro Noda	SON-2921	1782

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EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 11/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,748	NODA, KAZUHIRO	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06-02-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 06-02-2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

3. Figure 9,10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means"

and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because total word count exceeds 150.

Correction is required. See MPEP § 608.01(b).

Response to Amendment

6. **Status** Please all the replies and correspondence should be addressed to examiner's new art unit 2629. Receipt is acknowledged of papers submitted on February 19, 2004 under amendments and new claims, which have been placed of record in the file. Claims 1-12 are pending in this action.

7. The amendment filed 12-22-2005 does not introduces any new matter into the disclosure. The added material which is supported by the original disclosure.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4,7-9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (6,670,944 B1) in view of Sipvey et al. (5,886,353).

Regarding Claims 1-4,7-9 and 12 Ishi teaches a display device (Col. 7, Line 65, Col. 14, Line 1 to Col. 15, Line 39, Col. 16, line 59 to Col. 17, Line 38, Col. 11, Line 6 to Col. 12, Line 46, see figures 1-7) having: a plurality of pixels arrayed two-dimensionally (Col. 9, Lines 44-48, 59); and a scanner for selecting each of said plural pixels column by column or row by row (Col. 10, Lines 7-14); wherein said scanner is composed of a shift register (Col. 10, Lines 7-14) comprising a plurality of unit circuits cascade-connected to form a plurality of stages (see figure 7, Col. 14, Lines 4-6), each unit circuit having: a shifter (Col. 11, Line 32) comprising a NAND circuit (see figure 4-7, Col. 12, Line 30) to receive an input pulse as one input thereof; and a holder having a PMOS transistor and an NMOS transistor (Col. 8, Lines 13-19, Col. 12, Lines 30, 35,36, Col. 14, Lines 12-14, since the inverter does not transfer the received data until next clock cycle), which are connected in series between a power supply and a clock input end fed with a clock pulse (see figure 7, item 1562, Col. 14, Lines 6-10) and of which gates and drains are mutually connected in common respectively (Col. 13, Lines 49-53) wherein the input end of said holder is connected to the output end of said NAND circuit (see figure 7, Col. 14, lines 21-25), and the output potential thereof is fed as another input to said NAND circuit (see figure 7, Col. 14, Lines 1-5, Lines 21-39); and the odd-stage unit circuits and the even-stage unit circuits operate in synchronism respectively with clock pulses (Col. 14, Line 1 to Col. 15, Line 39, Col. 16, Line 59 to Col. 17, Line 38, Col. 11, Line 6 to Col. 12, Line 46) having a 1/4 phase

difference from each other (Col. 8, Lines 6-40, teaches N-phase = 6 such that phase difference is 1/6 however, N is an arbitrary number and when N=4 phase difference is 1/4).

However, Ishi fails to recite a sample and hold circuitry. However, Spivey et al. teaches a sample and hold circuitry (Col. 4, Lines 61-65, Col. Figure 8, Col. 6, Lines 40-57) and a PMOS transistor connected in parallel with the NMOS transistor in said holder and receiving, as a gate input thereto, a pulse opposite in phase to the input pulse fed to said holder (Col. 4, Lines 61-65, see figures 6,8,21,22,23A and 23B, Col. 6, Lines 40-57, Col. 18, Lines 5-29). The reason to combine is Spivey et al. teaches using of CMOS technology using N-channel and P-channel devices, which produces a better circuit performance as well as design flexibilities in an imaging device application (Col. 2, Lines 49-52). Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate teaching of Spivey et al. in teaching of Ishi to be able to have a an image displaying unit with sample and hold circuitry using of CMOS technology using N-channel and P-channel devices, which produces a better circuit performance as well as design flexibilities in an imaging device application; and easy to fabricate with reduce power consumption.

Regarding Claims 4 and 9, Ishi teaches an inverter circuit, which inverts the phase of the input pulse fed to said holder (Col. 8, Lines 13-19) and then feeds the phase-inverted pulse to the gate of said PMOS transistor (Col. 8, Lines 25-30, Col. 9, Lines 48-53).

Regarding Claim 12, Ishi teaches plurality of pixel display elements are liquid crystal cells (Col. 9, Lines 42-65).

9. Claims 5,6,10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (6,670,944 B1) in view of Sipvey et al. (5,886,353) as applied to claims 7-9,12 above, and further in view of Sekine (6,930,665 B2).

Regarding Claim 5,6,10, and 11, Ishi modified by Spivey et al. teaches the input pulse in synchronism with the clock pulse having a 1/4 phase difference from the clock pulse fed to said holder and then feeds pulse to said shifter and an inverter circuit for inverting the phase of said input pulse and feeding the phase-inverted pulse to said waveform shaping shift circuit (Col. 16, lines 32-55, Col. 8, Lines 4-40, teaches N-phase = 6 such that phase difference is 1/6 however, N is an arbitrary number and when N=4 phase difference is 1/4). However, Ishi modified by Spivey et al. fails to disclose waveform shaping shift circuit. However, Sekine teaches, waveform shaping shift circuit.(Col. 12, Lines 4-21, Col. 12, Line 55 to Col. 13, Line 14). The reason to combine is Sekine teaching of wave shaping helps reduce influence of capacitances from signal line and produces accurate digital-analog conversion (Col. 2, Lines 30-39). Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate teaching of Sekine in teaching of Ishi modified by Spivey et al. to be able to have a an image displaying unit to have wave shaping capabilities so that reduce influence of capacitances from signal line and produces accurate digital-analog conversion and without increasing cost of the real estate, produce higher resolution in image displaying.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Uchino et al. (US 6,512,505 B1) Liquid Crystal Display apparatus, its driving method and liquid crystal display system..

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

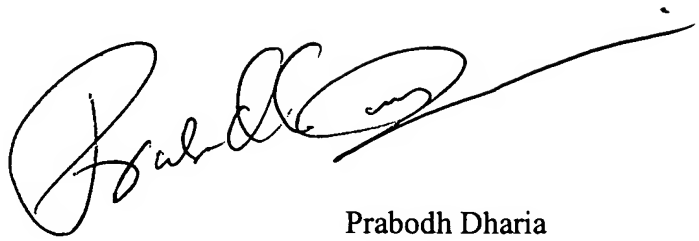
12. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231



Prabodh Dharia

Partial Signatory Authority Program

AU 2629

October 30, 2006